Intrinsic DC Operation and Performance Potential of 50nm Gate Length Hydrogen-terminated Diamond Field Effect Transistors

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The hydrogen-terminated diamond surface has demonstrated unique potential in the development of high power and high frequency field effect transistors (FETs) [1]. Further exploration into the intrinsic performance limitations and device operation as gate length is reduced however is essential in unveiling the potential of this exotic material system as a viable and competitive high power and high frequency device technology.

Progress and challenges involved with the scaling of hydrogen-terminated diamond FETs to sub-100nm gate dimensions have recently been reported [2,3]. In this work we describe the intrinsic operation and DC performance of devices at the 50nm node; the shortest gate length yet realised for an operational diamond FET.

50nm gate length devices were fabricated as illustrated in Fig. 1 using Element Six provided CVD grown (001) orientated single-crystal diamond. Devices were isolated electrically by selective removal of the hydrogen-termination with oxygen plasma. Sub-100nm gate length device yield and performance was improved substantially through fine optimization of the KI wet etch of the Au encapsulation layer which forms the ohmic contacts directly. The inherent ohmic contact edge roughness and large gate-ohmic separation associated with this process are therefore reduced. A Scanning Electron Microscope image of the resultant device structure is presented in Fig. 2.

Typical 50nm device output characteristics are presented in Fig. 3. Performance figures include a maximum drain current I_{dmax} ~ 300 mA/mm and a peak extrinsic transconductance g_m ~ 100 mS/mm. An increase in off-state output conductance is observed for larger magnitude V_{ds} as further verified upon inspection of device logarithmic transfer characteristics (Fig. 4). This short-channel type response results in an increase in sub-threshold swing (SS) and a shift in threshold voltage (V_{th}) from positive to negative as greater bias is applied between source and drain (Fig.5). Although electrostatic control of the drain current by the gate is reduced at more negative V_{ds}, a minimum I_{on}/I_{off} of ~ 1.5×10^4 is maintained across the inspected bias range indicating the ability to pinch off the drain current at a gate dimension 50nm. Fig. 6 demonstrates the degradation of I_{on}/I_{off} for increased magnitude source-drain voltage and fixed gate bias close to device pinch off.

Device intrinsic transconductance was determined by extraction of parasitic access resistances from low V_{ds} device on-resistance (R_{on}) which in turn was extracted directly from the linear response of device output characteristics (as shown in Fig. 3). Given the symmetric positioning of the gate contact between source and drain and accounting for the channel resistance beneath the gate, the total source resistance (R_s) was determined from this figure and the intrinsic transconductance then extracted by a similar process to that described in [3] to be ~ 660 mS/mm. A value of 8.8 Ω.mm was determined for R_s, of which 4.0 Ω.mm is attributed to ohmic contact resistance (R_c) as measured by TLM test structures and the remaining 4.8 Ω.mm to the lateral resistance through the diamond between source and gate (R_{s-g}). Utilising the sheet resistance figure of 10 kΩ/sq for the exposed diamond surface as measured by TLM, a source-gate separation of L_{s-g} ~ 480nm was determined for these devices.

Comparison between the intrinsic and extrinsic transconductance values of 660 mS/mm and 100 mS/mm respectively emphasizes the need to greatly reduce the total access resistance within these devices to better enable the potential performance of this technology. Fig. 7 demonstrates the impact of R_s upon extrinsic transconductance g_m at this gate dimension as it is increased to its intrinsic value at R_s = 0 Ω.mm. The individual components of R_s i.e. R_c and R_{s-g} are highlighted in addition to the dependency upon the source-gate contact separation L_{s-g}. It is observed that as L_{s-g} approaches zero, an increase in extrinsic transconductance up to a value approaching 200 mS/mm for a similar value of R_c = 4.0 Ω.mm should be attained.

In summary, although short channel effects have been observed in the operation of 50nm hydrogen-terminated diamond FETs, a minimum I_{on}/I_{off} figure of ~ 1.5×10^4 indicates pinch-off of the drain current is achievable at this gate dimension and across the inspected bias range. This is the first time the detailed intrinsic operation of diamond FETs with gate length below 100nm has been reported. Furthermore, deduction of the large intrinsic transconductance figure of 660mS/mm indicates substantial improvement in DC performance should result from further reduction to device access resistance and lead to substantial improvement in device high frequency performance for hydrogen-terminated diamond FETs with sub-100nm gate length.

[1] K. Ueda *et al, IEEE Electron Device Letters*, vol. 27, no. 7, pp. 570 – 572, July. 2006.
[2] D. A. J. Moran *et al*, doi:10.1016/j.mee.2010.11.029, *Microelectronic Engineering* (in press)
[3] David. A. J. Moran *et al*, *IEEE Electron Device Letters,* (accepted 9th Feb 2011 - in press)

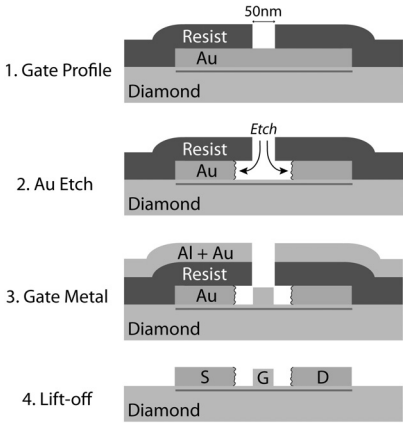

Fig. 1. Hydrogenated diamond FET fabrication process

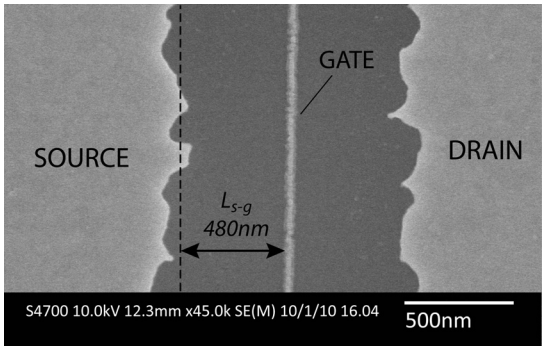

Fig. 2. SEM image of 50nm FET structure

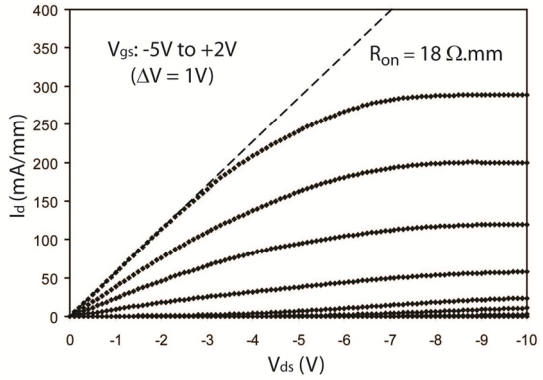

Fig. 3. 50nm device Output characteristics

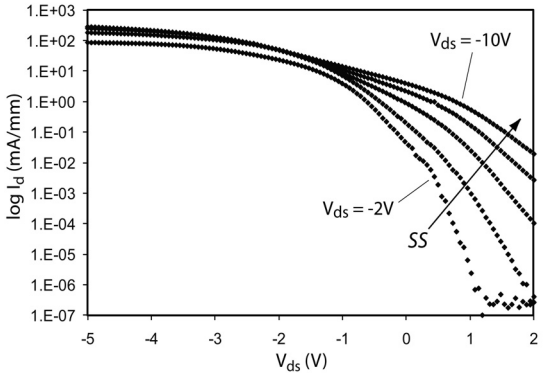

Fig. 4. 50nm device log Transfer characteristics

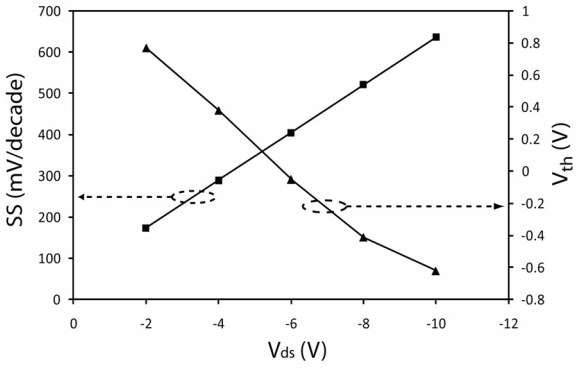

Fig. 5. Sub-threshold swing (SS) & threshold voltage (V_{th}) vs. V_{ds}

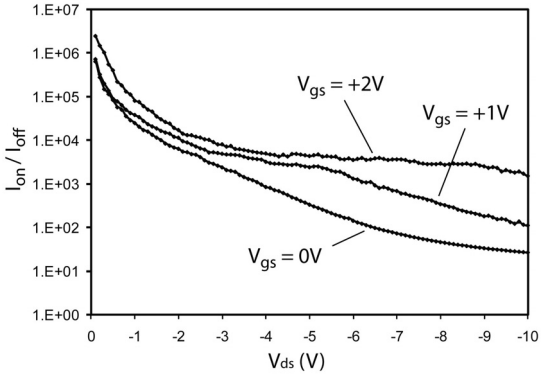

Fig. 6. I_{on}/I_{off} vs. V_{ds} for V_{gs} = 0V, +1V & +2V

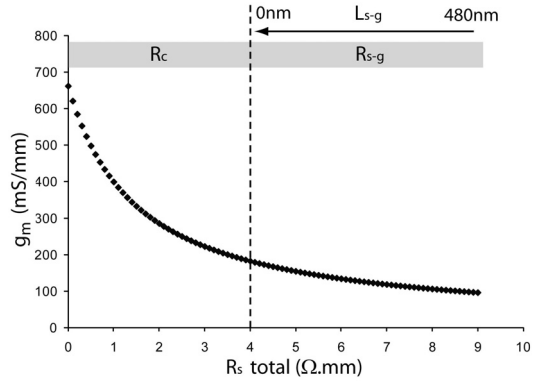

Fig. 7. Transconductance vs total source resistance. Contribution of contact resistance (R_c) and lateral access resistance (R_{s-g}) illustrated.