# Hydrogen-Terminated Diamond Field-Effect Transistors With Cutoff Frequency of 53 GHz

Stephen A. O. Russell, Salah Sharabi, Alex Tallaire, and David A. J. Moran

***Abstract*—Homoepitaxial diamond has been used to demonstrate the RF performance of 50-nm gate length hydrogen-terminated diamond field-effect transistors. An extrinsic cutoff frequency of 53 GHz is achieved which we believe to be the highest value reported for a diamond-based transistor. The generation of an RF small signal equivalent circuit is used to extract device elements to better understand variation between intrinsic and extrinsic operation. An intrinsic cutoff frequency of 90 GHz is extracted through this process, verifying the requirement to minimize access resistance to maximize the potential high-frequency performance of this technology.**

***Index Terms*—Field-effect transistor (FET), homoepitaxial diamond, hydrogen terminated, RF performance.**

## I. Introduction

As A wide-bandgap semiconductor (5.47 eV) [1] with high thermal conductivity ($> 20$ W/cm $\cdot$ K) [1], diamond is attractive for high-power device applications. A high intrinsic carrier mobility ($> 3000$ cm$^2$/V $\cdot$ s) [1] also suggests diamond as a promising material for high-frequency device operation. A concerted effort has been made over the last decade to produce RF operation field-effect transistors (FETs) utilizing the subsurface conductivity arising from the hydrogen termination of the diamond surface. Through the reduction of device gate dimension, the highest cutoff frequency ($f_T$) previously reported is 45 GHz for 100-nm and 150-nm gate length ($L_g$) technologies [2], [3] in comparison with 260 GHz for a leading GaN-based device [4]. This letter describes, for the first time, the RF operation of unpassivated 50-nm gate length diamond FETs and discusses the variation in intrinsic and extrinsic performance via equivalent circuit generation and analysis.

## II. Experiment

The material used in this work was chemical-vapor-deposited 4.7 $\times$ 4.7 mm (001)-oriented homoepitaxial diamond supplied by Element Six. Prior to the hydrogen termination of the diamond, a surface clean was undertaken in boiling aqua regia and then $H_2SO_4/HNO_3$ to remove any graphitic contaminants. Hydrogen termination was then performed in high-power hydrogen plasma for 30 min at 580 °C.

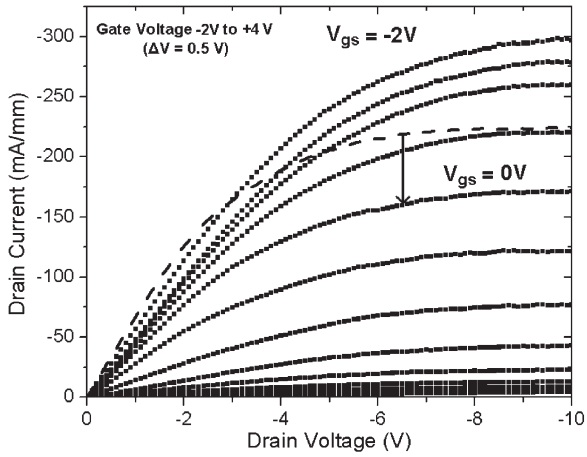


Fig. 1. DC output characteristics of a 50-nm gate length FET ($I_d$ versus $V_{\rm ds}$ with fixed $V_{\rm gs}$). The dashed line indicates initial measurement of $I_d$ prior to application of the presented gate voltage range.

Subsequent fabrication of the 50-nm gate length devices involved a three-step lithography process with a gold "sacrificial layer" employed to protect the hydrogen-terminated diamond surface during processing. This process is reported elsewhere [5] and is modified here to allow the formation of the coplanar waveguides required for RF device characterization. The device structure comprised a 2 $\times$ 25 $\mu$m two-finger layout with aluminum as the gate electrode contact material evaporated directly on to the hydrogen-terminated diamond surface. The definition of device geometry was achieved through oxygen plasma treatment to remove hydrogen termination and electrically isolate individual unpassivated devices.

## III. Results

Prior to device fabrication and post hydrogen-termination, atomic force microscopy was used to measure the diamond surface roughness to be $< 0.2$ nm RMS. A sheet resistance of $\sim$11 k$\Omega$/sq and a contact resistance of $\sim$5 $\Omega \cdot$ mm were extracted via transmission-line-model test structures. DC output current–voltage characteristics and transconductance response for a typical 50-nm device are presented in Figs. 1 and 2, respectively. The initial dc measurement with zero gate bias yielded a maximum drain current of 225 mA/mm at $-$10-V $V_{\rm ds}$. Subsequent measurement with a gate bias applied between $-2$ V and $+4$ V demonstrated good transistor action but led to a shift in drain current at zero gate voltage from the initial

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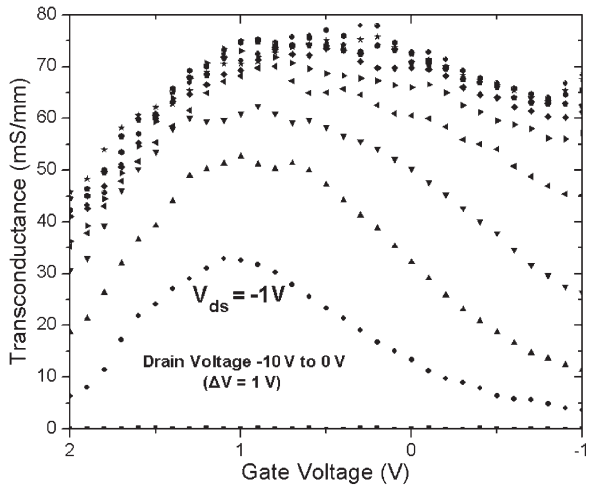


Fig. 2. Transconductance versus $V_{\rm gs}$ with fixed $V_{\rm ds}$ for a 50-nm gate length FET.

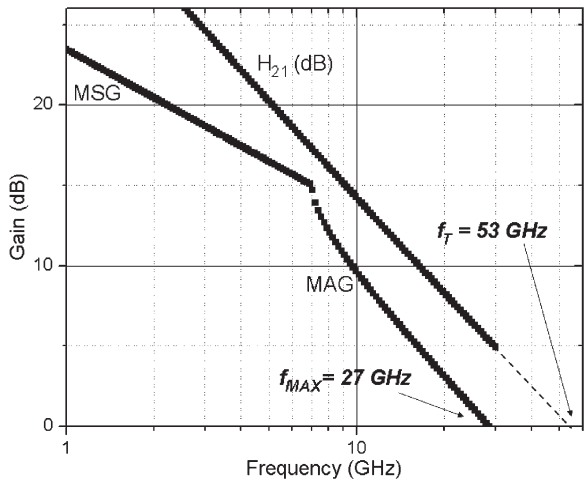


Fig. 3. $H_{21}$ and MSG/MAG versus frequency for a 50-nm gate length FET showing an extracted extrinsic $f_T$ of 53 GHz and $f_{\rm MAX}$ of 27 GHz.

measured 225 mA/mm to a reduced value of 170 mA/mm as shown in Fig. 1. A maximum drain current of 295 mA/mm was then measured at a gate bias of $-2$ V. Irreversible degradation in device performance was observed for gate bias less than $-2$ V in a similar manner to that reported elsewhere [6]. Following the initial degradation in drain current after the application of the presented gate voltage range, the device dc characteristics as represented in Fig. 1 remained sufficiently stable and repeatable to allow further dc and RF characterization. In comparison with previously reported device operation at this gate dimension, a substantial shift in threshold voltage is observed with these devices [5]. This may largely be attributed to the sensitivity of the hydrogen-terminated surface during processing.

The device gate leakage remained minimal with a peak value of 0.02 mA/mm measured across the inspected bias range. An extrinsic transconductance peak of 78 mS/mm was measured at a bias point of $+0.2$-V $V_{\rm gs}$ and $-8$-V $V_{\rm ds}$. This value is lower than that previously reported for submicrometer-gate-length devices and can be attributed to a process-associated increase in access resistance at this reduced gate dimension [5].

The RF measurement was performed at a bias point of $-0.4$-V $V_{\rm gs}$ and $-8$-V $V_{\rm ds}$ and small signal s-parameter data measured between 1 and 30 GHz. Despite the initial shift in the $I$–$V$ characteristics, transconductance plateaus and only marginally changes between $+1$ and $-1$ V $V_{\rm gs}$. Hence, this bias was chosen as an intermediate point to attempt to capture peak transconductance during RF measurement. Open and short on-wafer structures were employed to extract and remove parasitic elements arising from the coplanar waveguides. A de-embedded extrinsic $f_T$ value of 53 GHz was then extracted as determined from the device $H_{21}$ response shown in Fig. 3. An extrinsic maximum frequency of oscillation $(f_{\rm MAX})$ value of 27 GHz was similarly extracted from s-parameter data as shown in Fig. 3.

## IV. Discussion

Equations (1) and (2) describe the expressions for the intrinsic $f_T$ and $f_{\rm MAX}$ of a FET, respectively, where $g_m$ is the intrinsic RF transconductance, $C_g$ is the total intrinsic gate capacitance, i.e., $C_{\rm gs} + C_{\rm gd}$, $v$ is the average velocity of carriers underneath the gate (holes in this instance), $L_g$ is the gate length, $R_{\rm ds}$ is the output resistance, $R_g$ is the gate resistance, and $R_i$ is the intrinsic channel resistance [7]

$$f_T^{\rm int} = \frac{g_m}{2\pi.C_g} = \frac{v}{2\pi.L_g} \tag{1}$$

$$f_{\rm max}^{\rm int} = \frac{f_T^{\rm int}}{2}\left(\frac{R_{\rm ds}}{R_g + R_i}\right)^{\frac{1}{2}}. \tag{2}$$

TABLE I
Equivalent Circuit Elements

| $g_m$ (mS) | $C_{gs}$ (fF) | $C_{gd}$ (fF) | $R_s$ (Ω) | $R_d$ (Ω) | $R_{ds}$ (Ω) | $R_g$ (Ω) | $R_i$ (Ω) |
|---|---|---|---|---|---|---|---|
| 8.75 | 15.2 | 0.3 | 119 | 125 | 370 | 370 | 27 |

As originally discussed by Tasker and Hughes [8], the inspection of the equivalent FET circuit for $f_T$ extraction highlights the role of additional device elements in the reduction of the idealistic intrinsic $f_T$ figure to the measured extrinsic value. Equation (1) is then modified to include the impact of $R_{\rm ds}$ and the source and drain access resistances, $R_s$ and $R_d$, to describe the extrinsic $f_T$ as demonstrated in (3) [8]

$$f_T^{\rm ext} = \frac{\frac{g_m}{2\pi}}{[C_{\rm gs}+C_{\rm gd}].\left[1+\frac{(R_s+R_d)}{R_{\rm ds}}\right]+C_{\rm gd}.g_m.(R_s+R_d)}. \tag{3}$$

To investigate the variation between intrinsic and extrinsic device RF operation, a small-signal equivalent circuit model was obtained from s-parameter data. Table I shows the extracted equivalent circuit element values relevant to (1) and (2) from 50-nm gate length 50-$\mu$m-width FETs. An intrinsic $f_T$ of 90 GHz and an average carrier velocity of $2.82 \times 10^6 \pm 0.7 \times 10^6$ cm/s are calculated for these devices using (1). The error in carrier velocity is attributed to uncertainty in the exact effective gate length due to process-related line edge roughness of the gate contact. This value for carrier velocity is also less than that reported for larger gate length (200 nm to 1 $\mu$m) hydrogen-terminated diamond FETs of $\sim 4 \times 10^6$ cm/s [9].

The values for the output resistance $R_{\rm ds}$ and access resistances $R_s$ and $R_d$, presented in Table I, are found to reduce the extrinsic $f_T$ from the intrinsic value of 90 GHz to the measured value of 53 GHz ($\sim$59% of the intrinsic value). At a gate length of 50 nm, $R_{\rm ds}$ is low in comparison with an equivalent circuit value of 1800 $\Omega$ reported elsewhere for 100-nm gate length hydrogen-terminated diamond FETs [10]. This substantial increase in output conductance, perhaps attributed to short channel effects and/or increased interface state density at the diamond surface, leads to greater disparity between intrinsic and extrinsic $f_T$ at this gate dimension. Similarly, the device processing required to ensure sufficient yield of sub-100-nm gate length features leads to an increase in both source and drain access resistances, $R_s$ and $R_d$ [5], further contributing to the reduction in the FET extrinsic $f_T$ [11]. Although engineering of $R_{\rm ds}$ may not be feasible utilizing a conventional planar device structure, an improved $f_T$ may yet be achieved through better control and minimization of device access resistances.

Utilizing (2) and the relevant equivalent circuit values from Table I, an intrinsic $f_{\rm MAX}$ of 43 GHz is extracted for these devices. This can be compared with the measured extrinsic value of 27 GHz ($\sim$63% of the intrinsic value). Although it is difficult to derive a suitably accurate expression for the extrinsic $f_{\rm MAX}$ to allow similar analysis of intrinsic versus extrinsic operation [12], the impact of $R_g$, $R_i$, and $R_{\rm ds}$ on the intrinsic $f_{\rm MAX}$ can be seen upon inspection of (2). As with extrinsic $f_T$, a low $R_{\rm ds}$ limits the intrinsic $f_{\rm MAX}$ figure. The sum $R_g + R_i$ is also high in comparison to equivalent circuit values reported elsewhere for 100-nm T-gate devices ($R_g = 35\ \Omega$ and $R_i = 6.5\ \Omega$) with extrinsic $f_{\rm MAX}$ of 120 GHz [10]. Employing a T-gate structure to minimize the lateral gate resistance across the width of the device would reduce $R_g$ and greatly improve $f_{\rm MAX}$ in these devices. However, a comparatively low value for $R_{\rm ds}$ will still limit $f_{\rm MAX}$ at this gate length.

## V. Summary

The characterization of 50-nm gate length hydrogen-terminated diamond FET RF has been performed, yielding, to date, the highest reported cutoff frequency $(f_T)$ of 53 GHz for a diamond-based transistor. An equivalent circuit model has been produced from which average carrier velocity underneath the gate was extracted to be $2.82 \times 10^6$ cm/s. The measured $f_T$ value of 53 GHz is found to be only 59% of the intrinsic figure of 90 GHz as extracted from equivalent circuit data. Similarly, a reduction in $f_{\rm MAX}$ is observed with the extracted extrinsic value of 27 GHz only 63% of the intrinsic figure of 43 GHz. This significant suppression of high-frequency performance is attributed to a reduced output resistance and large access resistance, combined with a large gate resistance at this gate length. It is concluded that, although still limited by high output conductance, reduction in device access resistance and incorporation of a T-gate structure should yield significant further improvement in the high-frequency performance of sub-100-nm gate length hydrogen-terminated diamond FETs.

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